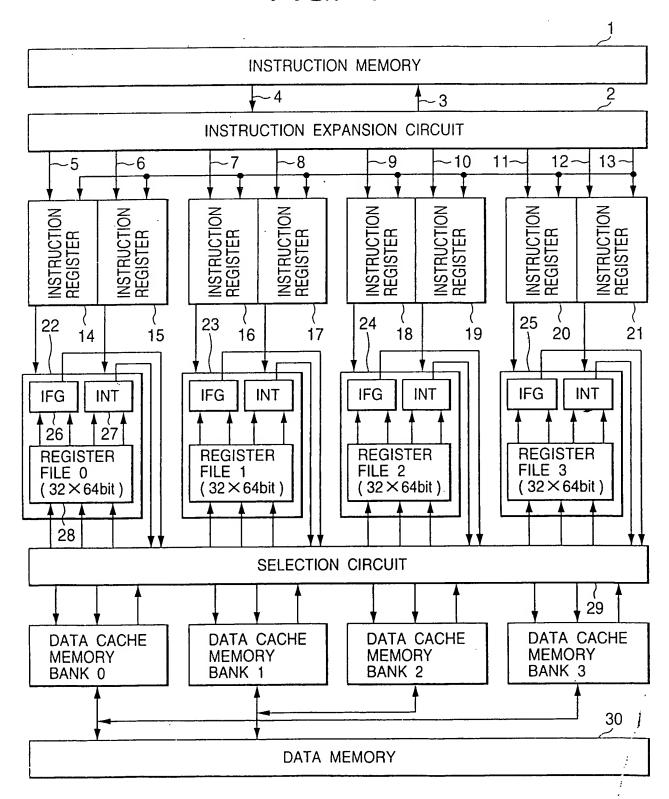
FIG. 1



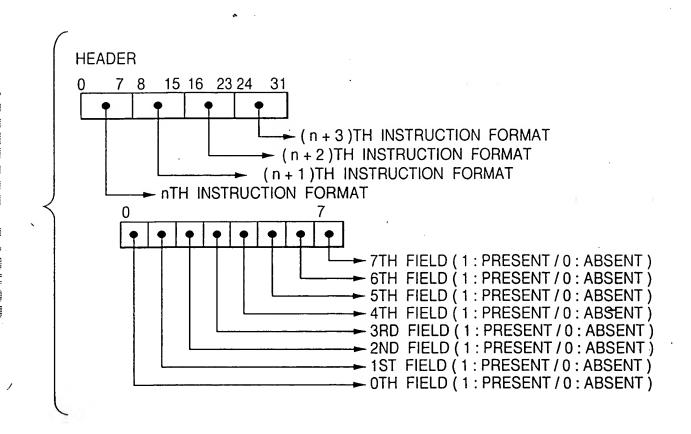
1=

Ш

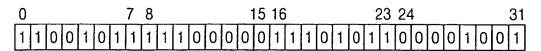
2/30 FIG. 2 SOURCE 1 S MODE SPARE SOURCE 0 (a) IFG FIELD 16 17 \ 21 22 26 8 11 12 SIMD / DEST. BANK | DESTINATION OPE. CODE IMMEDIATE 0 = > NORMAL MODE 0 = > CONTENT OF THE SOURCE 1 1 => SIMD MODE IS A REGISTER NO. 1 => CONTENT OF THE SOURCE 1 IS AN IMMEDIATE VALUE IMMEDIATE VALUE (0~31) (WHEN IMMEDIATE = 1) REGISTER NO. (0 ~ 31) **DESIGNATION OF** (WHEN IMMEDIATE = 0) OPERATIONS (256 KINDS MAX.) DEST. BANK (WHEN S MODE = 0) SAME WITH INT FIELD SIMD (WHEN S MODE = 1) DESIGNATE AN INSTRUCTION EXECUTED BY THREE OTHER BANKS 0 = > NOP1 => EXECUTE THE SAME INSTRUCTION CORRESPONDENCE BETWEEN THE BIT POSITION AND THE BANK CHANGES IN ACCORDANCE WITH THE INSTRUCTION REGISTER, AS SHOWN IN THE TABLE BELOW REGISTER CORRESPONDENCE BETWEEN SIMD POSITION OF NO. BIT POSITION AND THE BANK # THE INSTRUCTION I $(0 \sim 31)$ REGISTER 10 11 INSTRUCTION BANK 3 BANK 1 BANK 2 REGISTER 14 INSTRUCTION BANK 2 BANK 3 BANK 0 REGISTER 16 INSTRUCTION BANK 1 BANK 3 BANK 0 **REGISTER 18** INSTRUCTION BANK 1 BANK 2 BANK 0 **REGISTER 20 BRANCH TEST DEST. BANK** 18 19 23 24 31 13 14 11 10 DESTINATION SOURCE 1 OPE. CODE IMMEDIATE (b) INT FIELD SOURCE 0 000 = > BANK 0000 = > FAULSE001 => BANK 1 001 => TRUE IMMEDIATE VALUE (0 ~ 255) 010 = > BANK 2 010 = > BRANCH BANK REGISTER 2 (WHEN IMMEDIATE = 1) 011 = > BANK 3011 => BRANCH BANK REGISTER 3 REGISTER NO. (0~31) 100 = > BANK 4 100 = > BRANCH BANK REGISTER 4 (WHEN IMMEDIATE = 0) 101 => BANK 5 101 => BRANCH BANK REGISTER 5 110 => BANK 6 110 => BRANCH BANK REGISTER 6 111 => BRANCH BANK REGISTER 7 111 => BANK 7

AN EXAMPLE OF A PROGRAM STORAGE INTO THE INSTRUCTION MEMORY 31 0 FIELD 7 FIELD 1 HEADER 0 FIELD 0 FIELD 6 FIELD 0 FIELD 1 FIELD 4 63 32 FIELD 2 FIELD 4 FIELD 6 FIELD 7 FIELD 4 FIELD 2 FIELD 0 FIELD 1 95 67 64 FIELD 2 FIELD 3 FIELD 6 FIELD 4 FIELD 7 **HEADER 1** FIELD 0 FIELD 1 1ST INSTRUCTION (ADDRESS NOS. 4~23) 2ND INSTRUCTION (ADDRESS NOS. 24~35) 3RD INSTRUCTION (ADDRESS NOS. 35 ~ 59) 4TH INSTRUCTION (ADDRESS NOS. 60 ~ 67) 5TH INSTRUCTION (ADDRESS NOS. 72 ~ 79) 6TH INSTRUCTION (ADDRESS NOS. 80 ~ 87) 7TH INSTRUCTION (ADDRESS NOS. 88~91) 8TH INSTRUCTION (ADDRESS NOS. 92~95)

FIG. 4



HEADER 0



1 (n)TH INSTRUCTION FORMAT

0						255
FIELD 0 FIELD 1	NOP	NOP	FIELD 4	NOP	FIELD 6	FIELD 7

2 (n+1)TH INSTRUCTION FORMAT

0							- 255
FIELD 0	FIELD 1	FIELD 2	NOP	NOP	NOP	NOP	NOP

3 (n+2)TH INSTRUCTION FORMAT

0							255
FIELD 0	FIELD 1	FIELD 2	NOP	FIELD 4	NOP	FIELD 6	FIELD 7

4 (n+3)TH INSTRUCTION FORMAT

0	_						255
NOP	NOP	NOP	NOP	FIELD 4	NOP	NOP	FIELD 7

HEADER 1 15 16 S MODE = 15 (n)TH INSTRUCTION FORMAT · SIMD = 111 S MODE = 16 (n+1)TH INSTRUCTION FORMAT SIMD = 010255 NOP FIELD 2 FIELD 3 FIELD 2 FIELD 3 NOP NOP NOP S MODE = 17 (n+2)TH INSTRUCTION FORMAT SIMD = 101255 NOP NOP FIELD 6 NOP S MODE = 18 (n+3)TH INSTRUCTION FORMAT SIMD = 001255 FIELD 4 NOP NOP NOP NOP NOP FIELD 4 A FIELD DESIGNATING AN SIMD MODE A COPIED FIELD

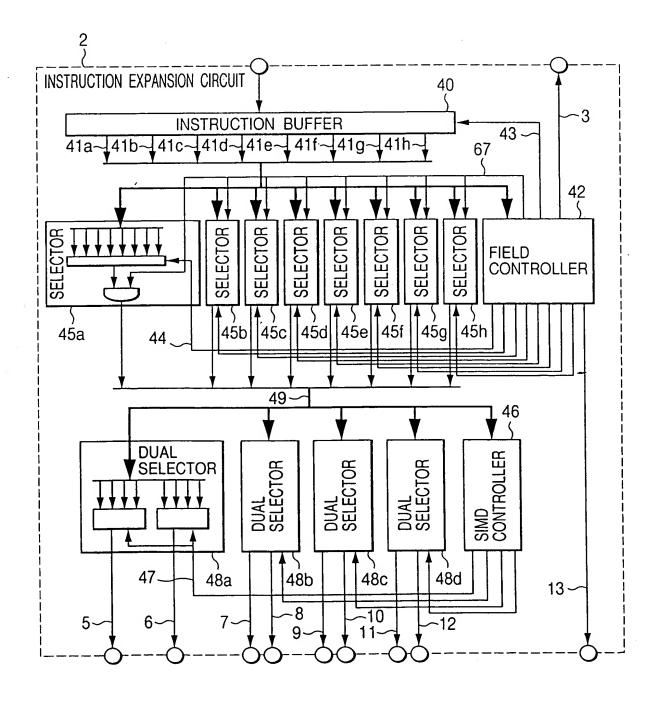
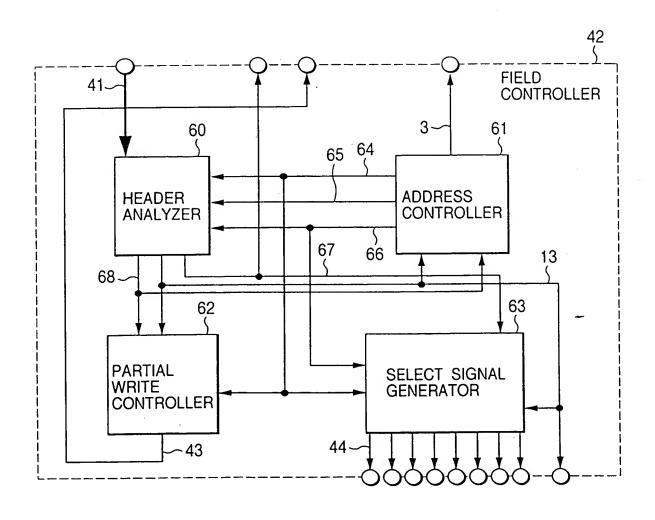


FIG. 8



AN EXAMPLE OF A PROGRAM STORAGE INTO THE INSTRUCTION MEMORY HEADER FIELD 0 FIELD 1 FIELD 4 FIELD 6 FIELD 7 FIELD 0 FIELD 1 32 FIELD 2 FIELD 0 FIELD 1 FIELD 2 FIELD 3 FIELD 4 FIELD 5 FIELD 6 72 FIELD 7 FIELD 0 HEADER FIELD 0 FIELD 1 FIELD 2 FIELD 3 FIELD 4 108 127 96 FIELD 1 FIELD 5 FIELD 6 FIELD 7 FIELD 2 FIELD 3 FIELD 4 FIELD 0

T0	T1	T2	T3	T4	T5	T6	T7	T8
IF.	EXP	EXE	WB	INSTRUCT	TON 1			
	IF	EXP	EXE	WB	INSTRUCT	TON 2		
INSTR	UCTION 3	IF	EXP	EXE	WB			
		UCTION 4	IF	EXP	EXE	WB	ļ	
		1	UCTION 5	IF.	EXP	//ÉXP2//	EXE	WB
				INSTR	UCTION 6	IF	EXP	EXE
REFETCH 0	SIGNAL 0	LINE 13	0	0	0	///:///	0	0
	TION LEN	GTH SIGN	AL LINE 6	8				_
0	24	12	32	4	36	////////	12	8
1	TION ADD			68	72	///108///	108	120
0	0	24	36	00	12	77799777	100	120
ADDRES:	32	56	68	100	104	136//	140	152
WRITE	NARLE BL	IS 43						-
11111111	11111100	10000011	11111111	01000000	11111111	100100000	00011100	00000011
DATA LA	TCHED IN	THE INST	TRUCTION DENCE W	BUFFER4 ITH FIG.9))			
							AHHH	
LICADED	ADDRESS	BUS 65						
neaven 0	0	1	2	3	0		1	2
FIELD 0	SELECT	SIGNAL 44)				1	
0	1	6	1	11	3			6
FIELD 1	2	7	2	-	4		3	-
FIELD 2	-	0	3	<u> </u>	5		4	
FIELD 3	<u> </u>	•	4	<u> </u>	6		5	
FIELD 4	3	-	5	<u> </u>	7			7
FIELD 5	-	-	6	•	0			
FIELD 6		<u> </u>	7	 	1	2	1 :	
FIELD 7	5		0	<u> </u>	•	1 2	<u> </u>	

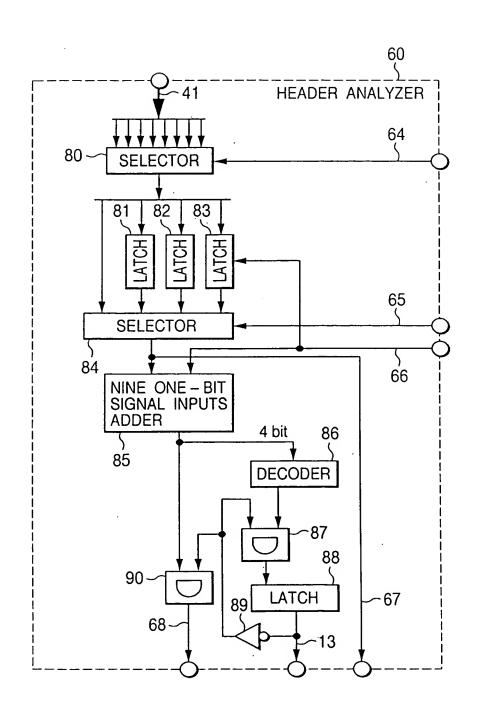
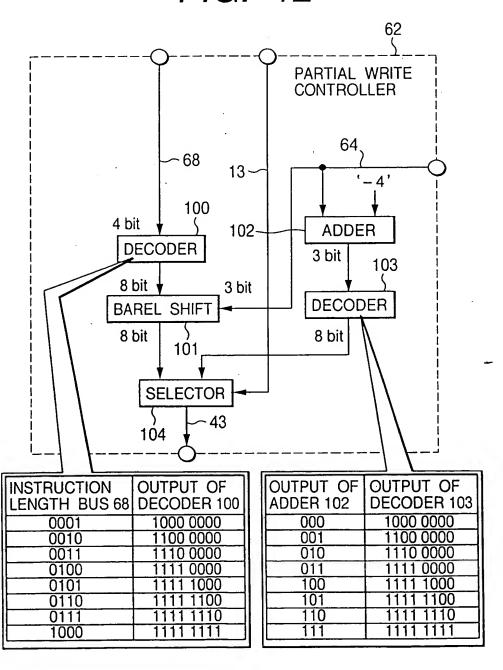
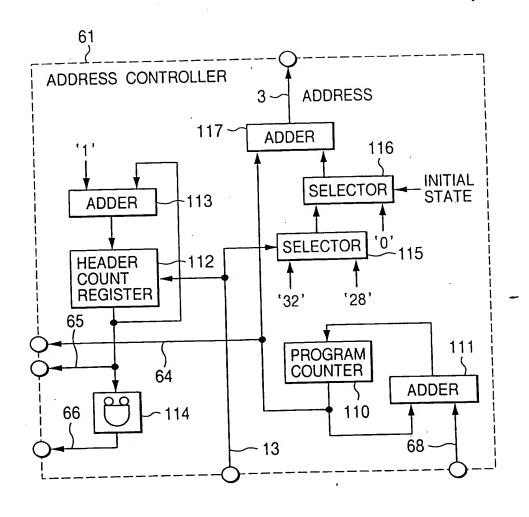
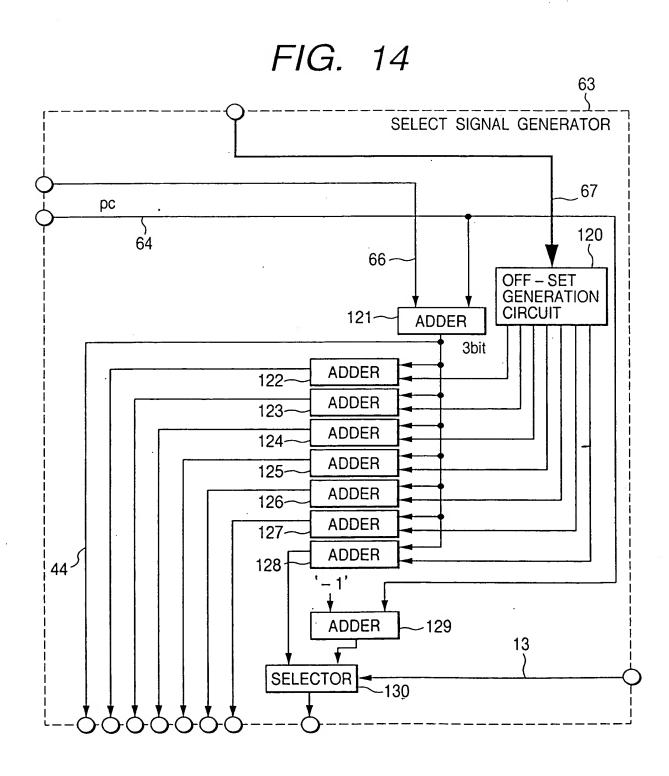


FIG. 12









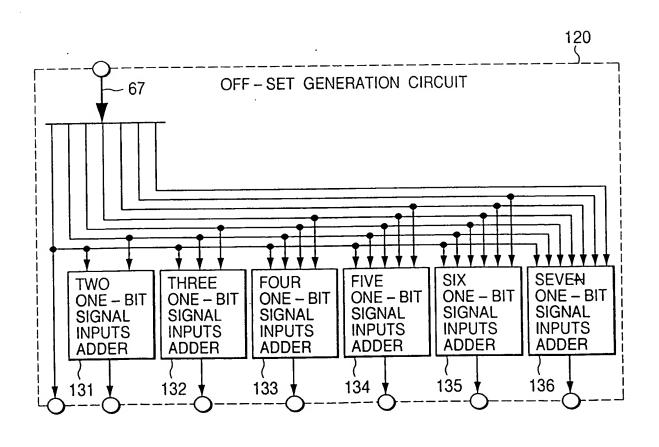


FIG. 16

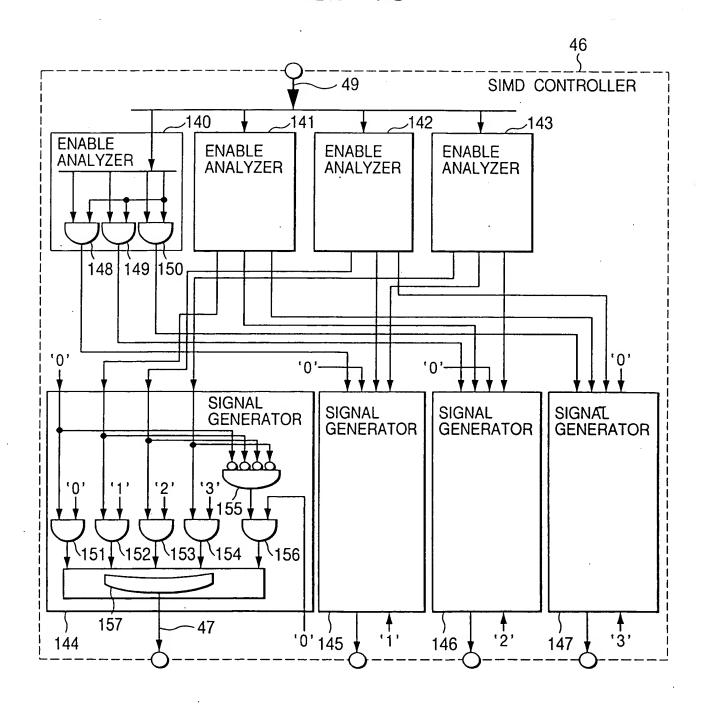
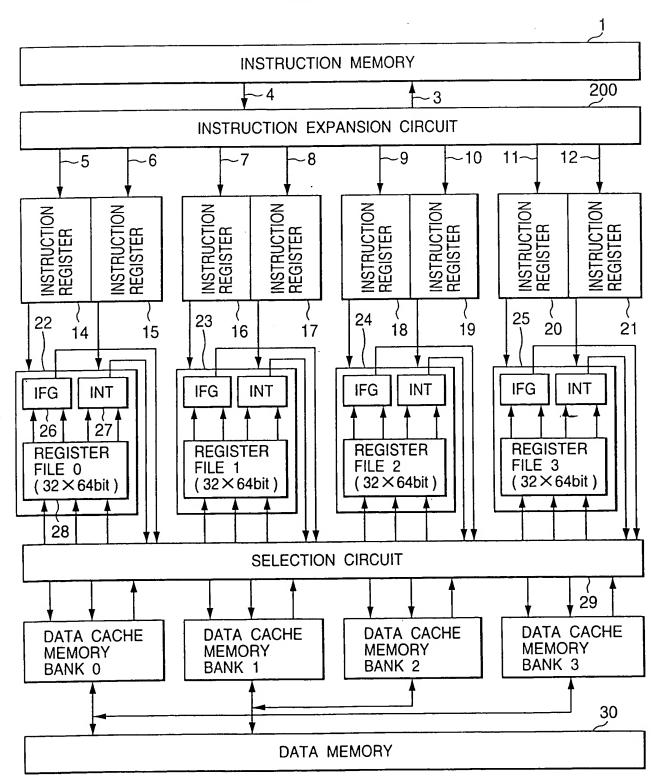


FIG. 17



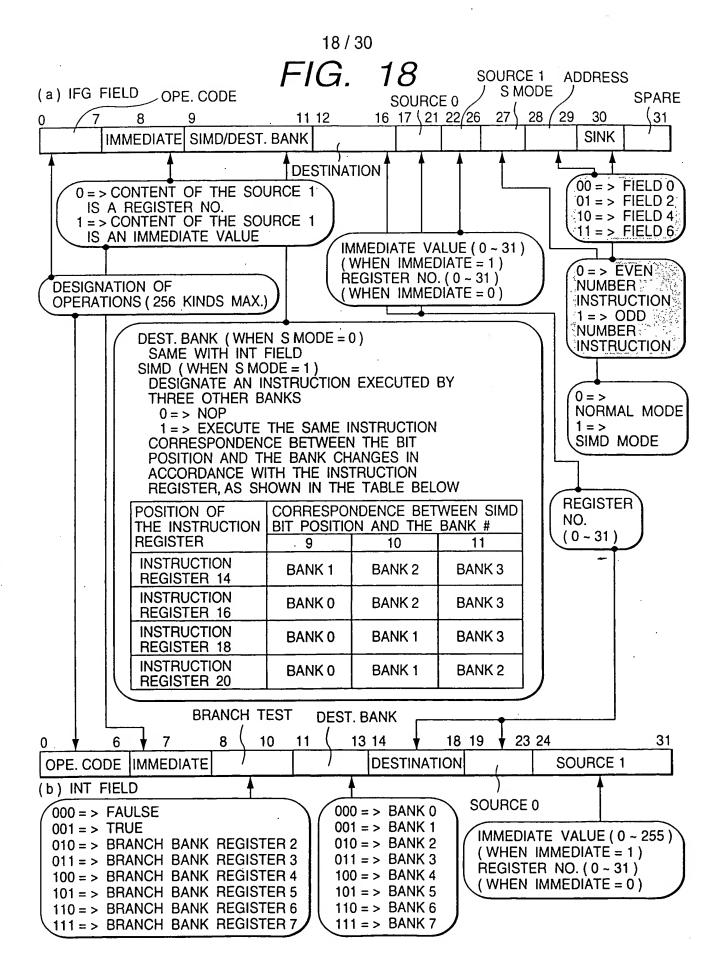


FIG. 19

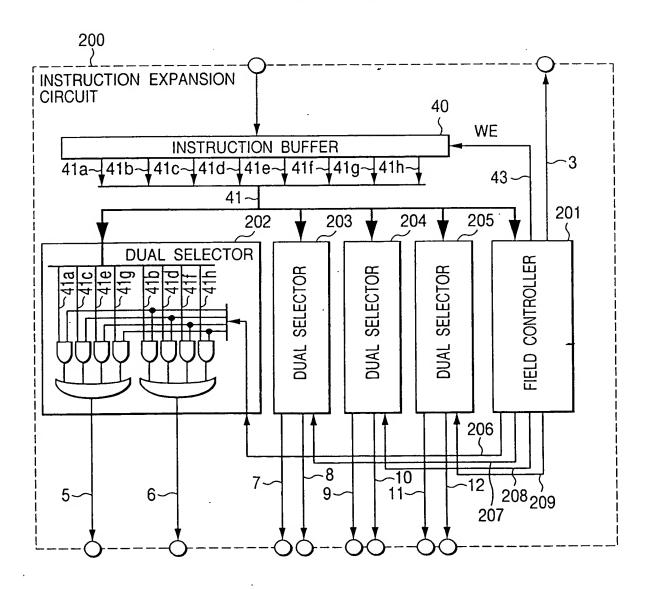
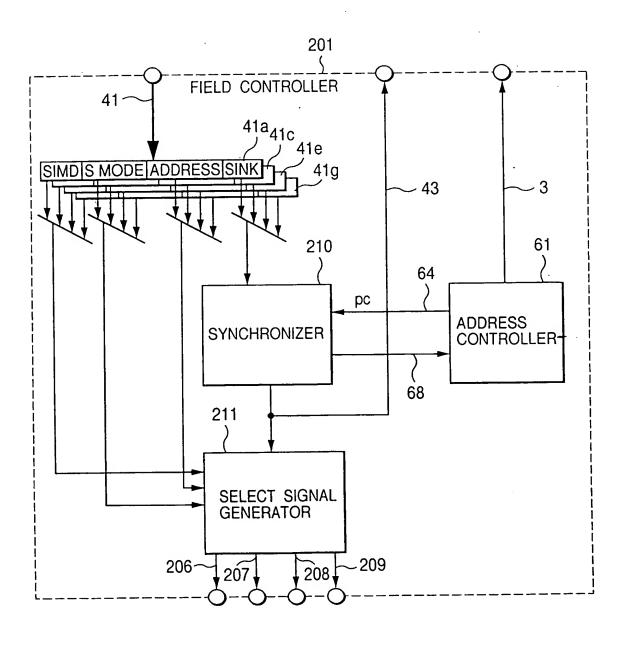


FIG. 20



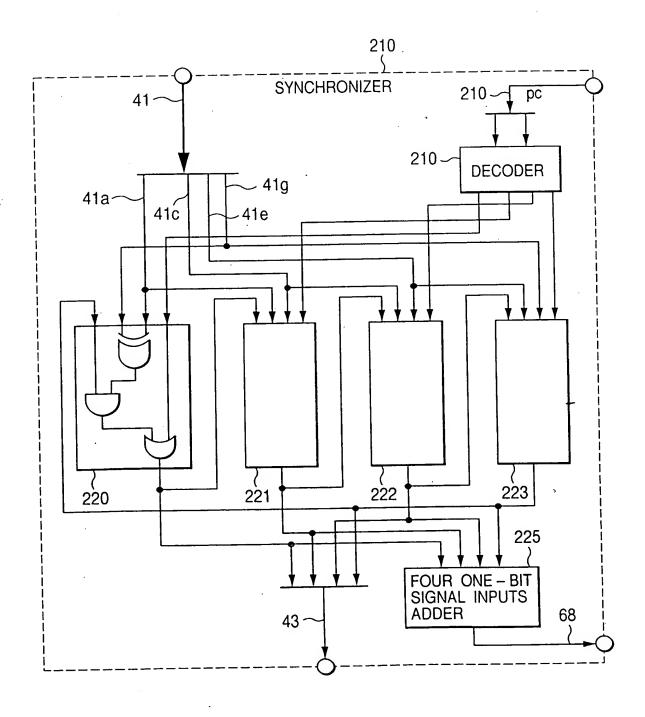


FIG. 22

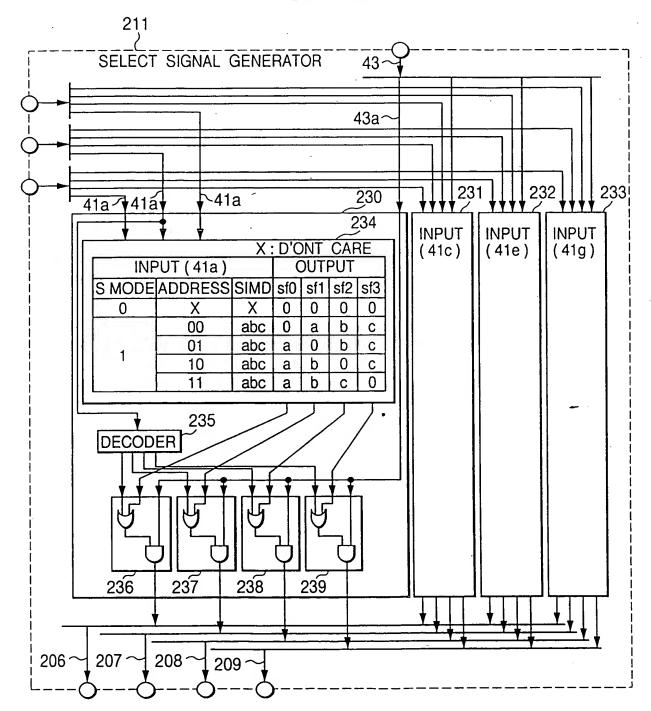
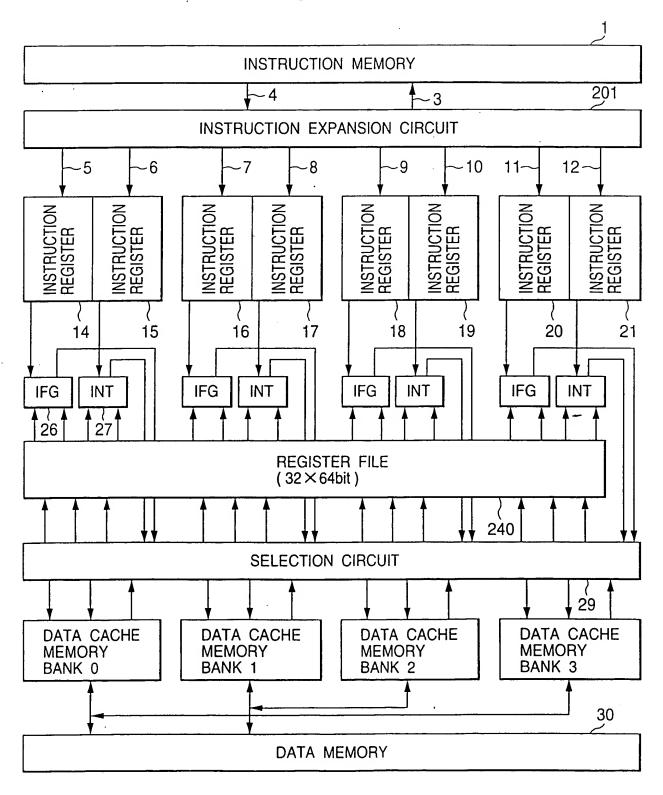
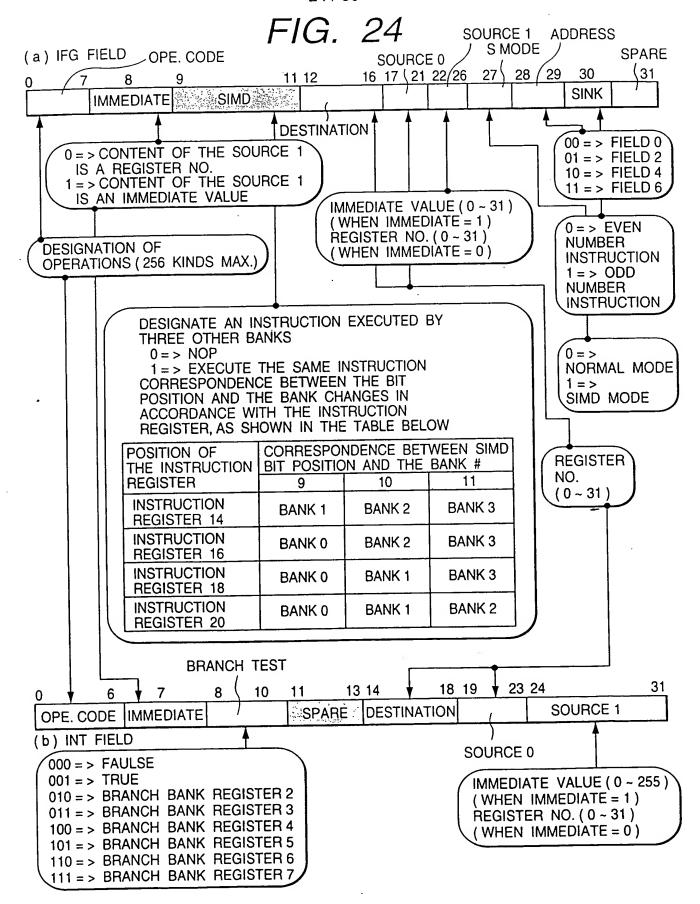
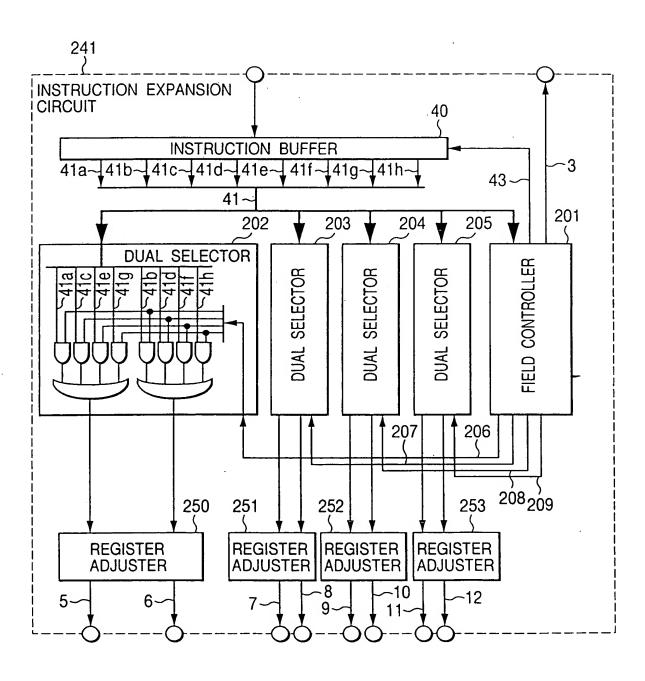


FIG. 23



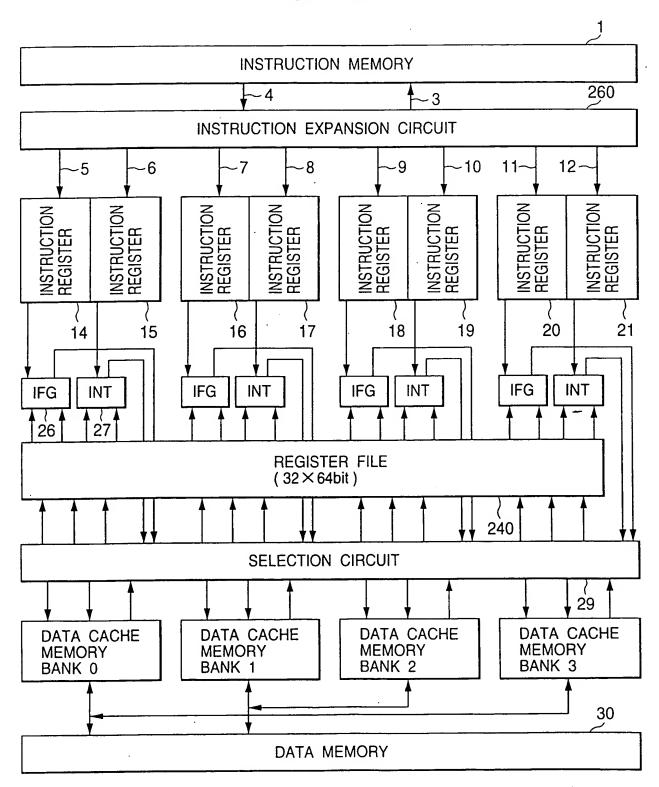
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	NPUT FIEL	OUTPUT FIELD	
SMODE	ADDRESS	REGISTER#	REGISTER#
0	X	N	N ·
	00	N	N
1	01	N	N + 3
	10	N	N + 2
	11	N	N + 1

FIG. 27



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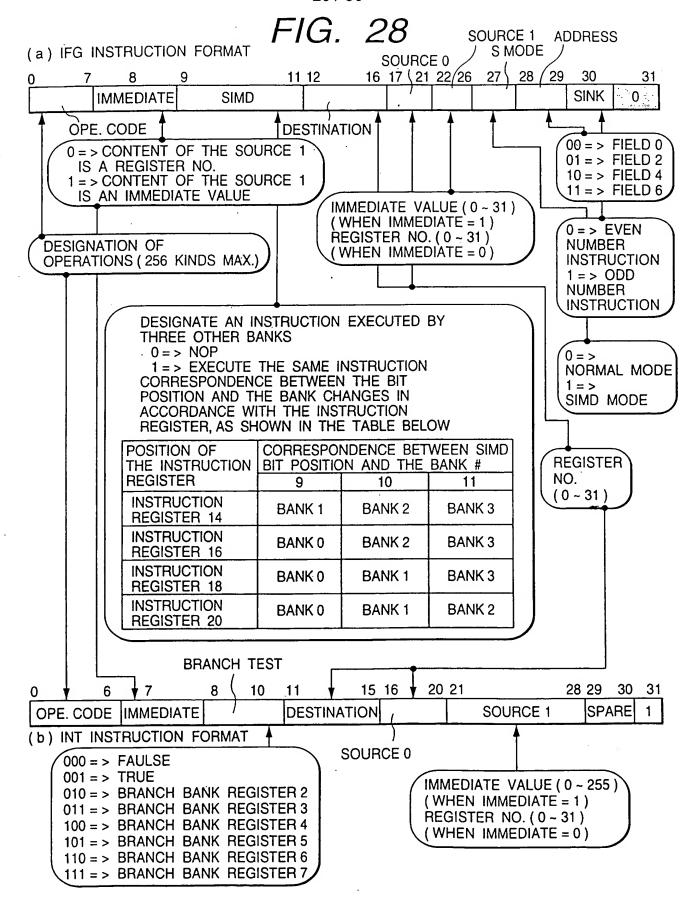


FIG. 29

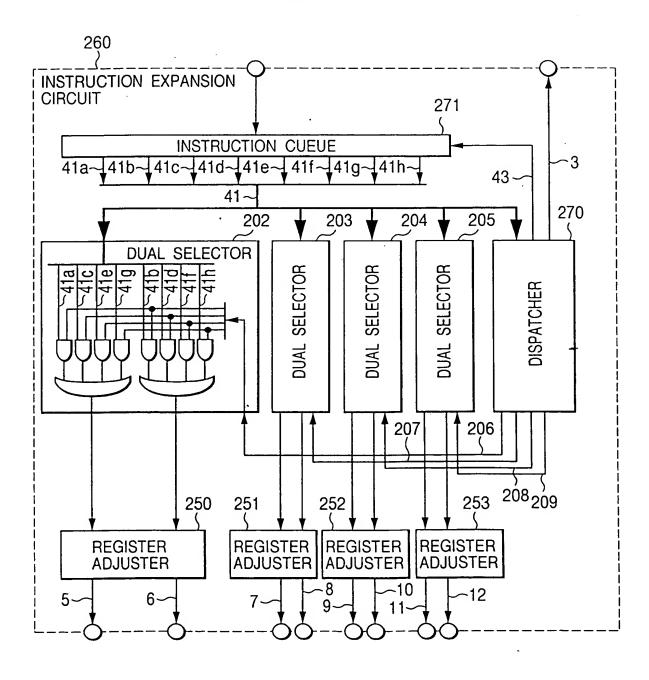


FIG. 30

